DATA SHEET

TDA8960
ATSC 8-VSB demodulator and decoder

Preliminary specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

ATSC 8-VSB demodulator and decoder TDA8960

FEATURES

General features

- One-chip Advanced Television Systems Committee (ATSC)-compliant demodulator and concatenated trellis (Viterbi)/Reed Solomon decoder with de-interleaver and de-randomizer
- 0.4 μm process
- 3.3 V device
- 64-lead QFP64 package
- Boundary scan test
- Output format: 8-bit wide bus.

8-VSB demodulator

- On-chip digital circuitry for tuner Automatic Gain Control (AGC)
- Square root raised cosine filter with 11.5% roll-off factor
- Fully internal carrier recovery loop
- Mostly internal clock recovery and AGC loops with programmable loop filters
- External indication of demodulator lock.

Adaptive equalizer

- Feed forward including a Decision Feedback Equalizer (DFE) structure
- Range of –2.3 to +10.5 μs
- Adaptation based on ATSC field sync (trained) and/or 8-VSB data (blind)
- Trellis (Viterbi) decoder
- Rate $^{2}/_{3}$ (Rate $^{1}/_{2}$ Ungerboeck code based).

Reed Solomon decoder

- (207, 187 and T = 10) Reed Solomon code
- Internal convolutional de-interleaving (I = 52; using internal memory)
- External indication of uncorrectable error; transport error indicator bit in Motion Picture Export Group (MPEG) packet header is also set
- Followed by de-randomizer based on ATSC standard.

I²C-bus interface

- I²C-bus interface to initialize and monitor the demodulator and Forward Error Correction (FEC) decoder. Operation without I²C-bus control is possible (default).

DOCUMENT REFERENCES

See the ATSC URL on ‘http://www.atsc.com’ for the following related documents:

- *“ATSC Digital Television Standard”* (document no. A/53, issued 1995 Sep 16)
- *“Guide to the use of the ATSC Digital Television Standard”* (document no. A/54, issued 1995 Oct 04).

APPLICATIONS

- Digital ATSC compliant TV receivers
- Personal computers with digital television capabilities
- Set-top boxes.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8960	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

GENERAL DESCRIPTION

The TDA8960 is an ATSC-compliant demodulator and forward error correction decoder for reception of 8-VSB modulated signals for terrestrial and cable applications:

- **Terrestrial:** reception of 8-VSB modulated signals via standard 6 MHz VHF/UHF terrestrial TV channels (TV channels 2 to 69 in the United States)
- **Cable:** reception of 8-VSB modulated signals via standard 6 MHz VHF/UHF cable TV channels.

Most of the loop components needed to recover the data from the received symbols are internal. The only required external loop components are a low-speed serial D/A converter and a Voltage Controlled crystal Oscillator (VCXO) for the symbol timing recovery and an opamp integrator for the AGC. Loop parameters of the clock and carrier recovery can be controlled by the I^2C-bus.

A tuner converts the incoming RF frequency to a fixed IF frequency centred at 44 MHz. The output of the tuner is filtered, followed by a down conversion in an IF block to a low IF frequency centred at $\frac{1}{2}$ the VSB symbol rate (or a frequency of approximately 5.38 MHz). The low IF signal is applied to the A/D converter.

To use its full input span, the A/D converter is located within what is typically a fine AGC loop which includes a variable gain stage at the output of the IF block. However, it is also possible to apply the TDA8960 AGC control output directly to the tuner. The detector for the TDA8960 AGC output is located after the A/D converter and determines the peak level of the incoming signals. After gain control, the low IF signal is sampled at a nominal rate of twice the VSB symbol frequency, or approximately 21.5 MHz.

The carrier recovery is performed completely internally. This function consists of a digital frequency and Frequency Phase-Locked Loop (FPLL).

Data shaping is performed with a square root raised cosine (half Nyquist) filter with roll-off factor of 11.5%.

Symbol timing recovery is performed mostly within the TDA8960, except that a low cost D/A converter and VCXO are required externally to generate the nominal 21.52 MHz clock signal for the A/D converter and TDA8960.

After carrier recovery, half Nyquist filtering and symbol timing recovery, adaptive equalization is performed based on the use of the ATSC field sync (trained equalization) and/or the 8-VSB data itself (blind equalization). The adaptive equalizer uses a DFE structure.

After trellis decoding, the stream is de-interleaved with a convolutional de-interleaver (interleaving depth 52). The memory for de-interleaving is on-chip. The Reed Solomon decoder is ATSC-compliant with a length of 207 and can correct up to 10 bytes. The decoded stream is de-randomized using a Pseudo Random Bit Sequence (PRBS). Finally the data is passed to a First-In, First-Out (FIFO) register that prevents the appearance of irregular gaps in the output data.

The output of the TDA8960 is an ATSC-compliant MPEG-2 packet stream together with a clock. Furthermore some signal flags are provided to indicate the sync bytes and the valid data bytes. Uncorrected blocks are also indicated.

The 8-bit wide MPEG-2 stream can be applied to an MPEG-2 transport demultiplexer.

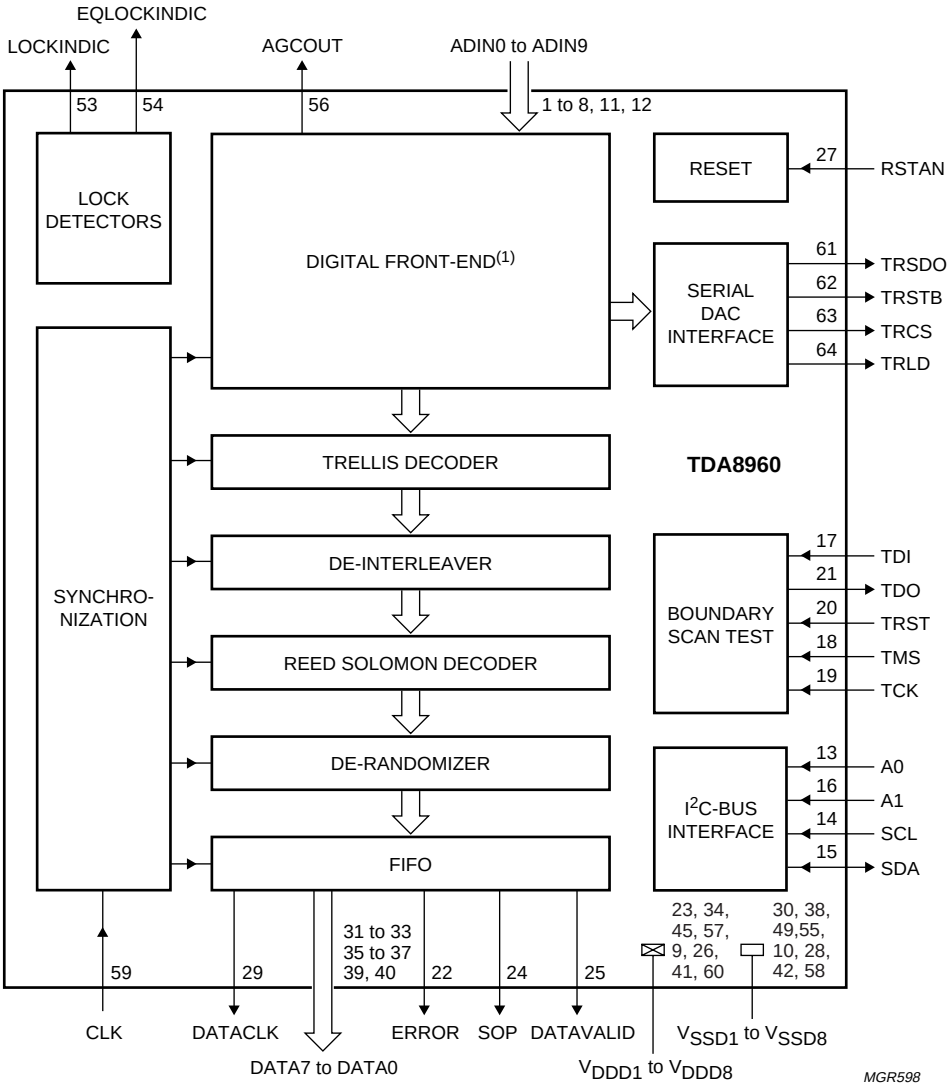
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
$I_{DDD(tot)}$	total digital supply current	V_{DDD} = 3.3 V	–	300	–	mA
f_{clk}	clock frequency		–	21.52	–	MHz
f_{sym}	symbol frequency		–	10.76	–	Msymbols/s
IL	implementation loss		–	–	–	dB
α_{ro}	half Nyquist filter roll-off factor		–	11.5	–	%
t_{acq}	acquisition time	note 1	–	–	290	ms
T_{amb}	ambient temperature		–20	–	+70	°C
P_{tot}	total power dissipation		–	1.0	–	W

Note

1. This corresponds to 12 training sequences.

BLOCK DIAGRAM



(1) The digital front-end consists of the following circuits:
- Fine AGC
- Carrier recovery
- Half Nyquist filter
- Symbol timing recovery
- Sync recovery and pilot removal
- Adaptive equalization.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
ADIN0	1	I	data input bit 0 from ADC
ADIN1	2	I	data input bit 1 from ADC
ADIN2	3	I	data input bit 2 from ADC
ADIN3	4	I	data input bit 3 from ADC
ADIN4	5	I	data input bit 4 from ADC
ADIN5	6	I	data input bit 5 from ADC
ADIN6	7	I	data input bit 6 from ADC
ADIN7	8	I	data input bit 7 from ADC
V_{DDD5}	9	–	digital supply voltage 5 (3.3 V)
V_{SSD5}	10	–	digital core ground 5
ADIN8	11	I	data input bit 8 from ADC
ADIN9	12	I	data input bit 9 from ADC
A0	13	I	I^2C-bus slave address bit 0
SCL	14	I	I^2C-bus clock
SDA	15	I/O	I^2C-bus serial data
A1	16	I	I^2C-bus slave address bit 1
TDI	17	I	TAP controller data input; note 1
TMS	18	I	TAP controller test mode select; note 1
TCK	19	I	TAP controller test clock; note 1
TRST	20	I	TAP controller asynchronous reset; note 1
TDO	21	O	TAP controller test data output (3-state); note 1
ERROR	22	O	transport packet block error signal
V_{DDD1}	23	–	digital supply voltage 1 (3.3 V)
SOP	24	O	start of transport packet signal
DATAVALID	25	O	transport packet data valid signal
V_{DDD6}	26	–	digital supply voltage 6 (3.3 V)
RSTAN	27	I	asynchronous reset
V_{SSD6}	28	–	digital ground 6
DATACLK	29	O	transport interface data clock
V_{SSD1}	30	–	digital ground 1
DATA7	31	O	transport packet data output bit 7
DATA6	32	O	transport packet data output bit 6
DATA5	33	O	transport packet data output bit 5
V_{DDD2}	34	–	digital supply voltage 2 (3.3 V)
DATA4	35	O	transport packet data output bit 4
DATA3	36	O	transport packet data output bit 3
DATA2	37	O	transport packet data output bit 2
V_{SSD2}	38	–	digital ground 2
DATA1	39	O	transport packet data output bit 1
DATA0	40	O	transport packet data output bit 0

SYMBOL	PIN	I/O	DESCRIPTION
V_{DDD7}	41	–	digital supply voltage 7 (3.3 V)
V_{SSD7}	42	–	digital ground 7
n.c.	43		not connected
n.c.	44		not connected
V_{DDD3}	45	–	digital supply voltage 3 (3.3 V)
n.c.	46		not connected
n.c.	47		not connected
n.c.	48		not connected
V_{SSD3}	49	–	digital ground 3
n.c.	50		not connected
n.c.	51		not connected
n.c.	52		not connected
LOCKINDIC	53	O	lock indicator of front-end
EQLOCKINDIC	54	O	lock indicator of equalizer
V_{SSD4}	55	–	digital ground 4
AGCOUT	56	O	AGC control signal (3-state)
V_{DDD4}	57	–	digital supply voltage 4 (3.3 V)
V_{SSD8}	58	–	digital ground 8
CLK	59	I	clock
V_{DDD8}	60	–	digital supply voltage 8 (3.3 V)
TRSDO	61	O	serial data to DAC
TRSTB	62	O	strobe signal to DAC
TRCS	63	O	chip select signal to DAC
TRLD	64	O	load signal to DAC

Note

1. In accordance with the *"IEEE 1149.1"* standard; pads TCK, TDI, TMS and TRST are input pads with an internal pull-up transistor and pad TDO is a 3-state output pad.

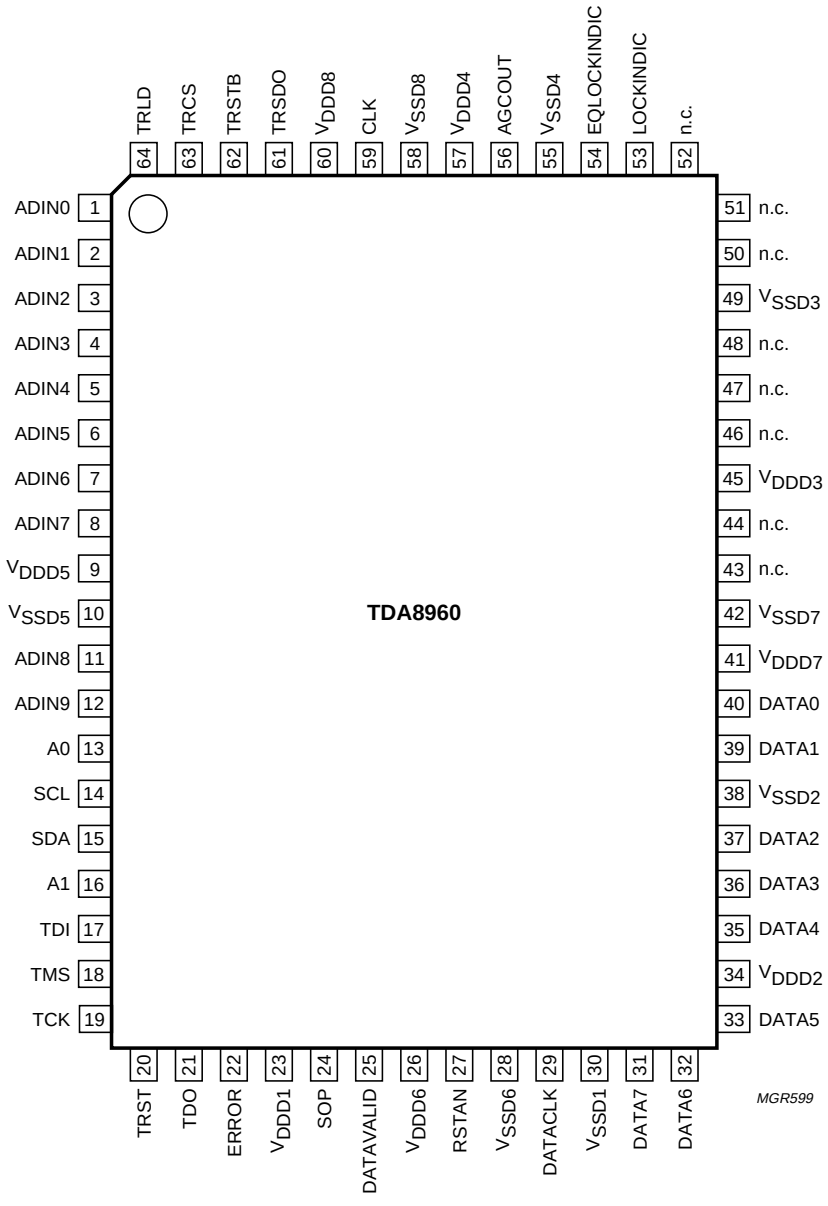


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The internal architecture of the TDA8960 consists of basically two parts:

- The front-end containing the AGC, carrier recovery, half Nyquist filter, symbol timing recovery, sync recovery and adaptive equalization
- The back-end containing the trellis decoder, de-interleaver, the Reed Solomon decoder and de-randomizer.

AGC

This block controls an analog gain over a range of up to ±20 dB.

The data from the A/D converter (Philips Semiconductors' TDA8763 is recommended) arrives at the VSB demodulator via inputs ADIN9 to ADIN0, which is10-bit wide. The format of the incoming samples can be programmed using the I^{2}C-bus accessible register 08H. By writing to bit 3 the format can be either twos complement or binary.

The absolute value of the input signal is averaged over several samples. The filtered signal is compared to a threshold. The threshold consist of a 4-bit signed value which can be programmed using the I^{2}C-bus. The 3-state output signal charges or discharges an off-chip ideal integrator and is used to control the gain controller of the tuner front-end module. The values of the signal are shown in Table 1.

Table 1 AGC output

PIN AGCOUT	COMMENT
1	output of the filter is smaller than the threshold
0	output of the filter is larger than the threshold
Z	output of the filter is equal to the threshold

The analog low-pass filter or integrator circuit should be designed with an 8 ms time constant. The response of the gain amplifier is linear with respect to the control voltage over the desired range of operation.

Carrier recovery

This circuit recovers the frequency and phase of the pilot carrier. The spectrum during the carrier recovery is displayed in Fig.3.

By default the carrier is present at 2.69 MHz. During carrier recovery a shift is applied such that the pilot is present at DC. It can happen that the pilot is present at the higher edge of the VSB spectrum. In this event the CR_INV bit in I^{2}C-bus register 08H (see Table 13) can be set to make sure that after the shift the pilot is at DC.

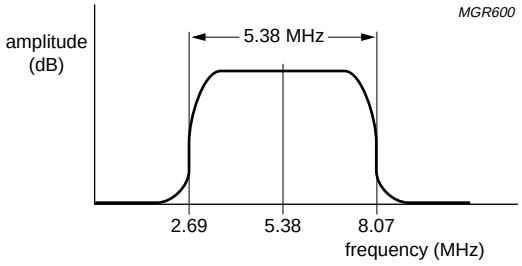


Fig.3 Signal spectrum during carrier recovery.

The carrier recovery is capable of tracking a frequency offset of up to 100 kHz from the nominal frequency offset within 100 ms.

By means of I^{2}C-bus read register 03H the current frequency offset in the carrier recovery can be read. This value can be used for fine tuning applications.

Sync recovery and pilot removal

This block performs several functions including pilot removal, segment and field sync removal and rescale AGC based on the segment sync. If this block is able to find a data segment sync signal, the external pin LOCKINDIC is asserted. The value of this signal can also be read through I^{2}C-bus control.

Adaptive equalization

The equalizer consists of a forward filter and a feedback filter section. Demodulated symbols from the synchronization and pilot removal block are received every symbol period. The equalizer tries to invert the effects of the channel on the transmitted symbol stream by filtering these symbols. The coefficients of the filters are updated every symbol period using the training sequence. There is also a provision to perform blind equalization. The filtered output is available for the next block, the trellis decoder.

The equalizer has been designed to correct a maximum pre-echo of 2.32 μs and a maximum post-echo of 10.50 μs. The equalizer uses an overlapping DFE to reduce the effects of co-channel interference.
The equalizer has been optimized to have a typical acquisition time of 12 training sequences, which corresponds to approximately 290 ms. The acquisition time has been defined as the time when the output signal-to-noise ratio reaches the Threshold Of Visibility (TOV). The ATSC defines a TOV of 14.9 dB for 8-VSB.

Based on the training signal and the output of the equalizer the Mean Square Error (MSE) signal is generated. This 16-bit value is used to control the channel adaptation process and is available though I^2C-bus control.

Control

The TDA8960 contains a complicated finite state machine. This state machine controls the sequence of operations that must be performed when a valid VSB data signal is detected in order for it to be properly decoded into a stream of MPEG-2 transport packets. The following steps have to take place:

1. The external tuner is directed to lock to a specified channel frequency. A VSB signal is present.
2. The tuner AGC locks to an acceptable signal gain.
3. The coarse AGC of the TDA8960 locks to acceptable A/D converter gain.
4. The timing and carrier recovery loops lock to the symbol clock and the carrier frequency.
5. The segment sync pattern is detected. The segment sync lock is acquired.
6. The fine AGC locks.
7. The field sync pattern is detected. The MSE of the received field sync training sequence is determined.
8. The equalizer uses subsequent training sequences to adapt itself to the channel conditions.
9. The equalizer adapts to the point that the MSE of the training sequence is sufficiently small. The trellis decoding, convolutional de-interleaving and Reed Solomon decoding processes all begin.
10. Valid MPEG-2 transport packets are generated.

The finite state machine consists of three states. After a reset has been applied, the state machine starts in state 0.

STATE 0: CHANNEL ACQUISITION

In this state either no channel signal is present or a channel signal is being acquired. The AGC, timing recovery and carrier recovery loops must first lock onto it. If the segment sync lock is lost, pin LOCKINDIC is LOW, or a hardware reset is applied to the VSB demodulator, the finite state machine returns to state 0.

STATE 1: EQUALIZER TRAINING

The finite state machine remains in state 1 until the MSE of the equalized training sequence falls below a certain threshold. It should be noted that in state 1 the back-end is continuously reset to make sure that after the demodulator has locked onto a signal, the trellis decoder and following processing blocks begin at the start of the next complete data field. By means of I^2C-bus registers 01H and 02H the MSE value of the equalizer can be read. This value can be used for applications such as antenna pointing.

STATE 2: NORMAL OPERATION

Normally the state machine would remain in state 2 as long as no synchronization error occurs. If the MSE of the equalized training sequence is exceeded for more than 100 ms, the equalizer is reset for one symbol period and the adaptation process starts again. If the demodulator is in this state, the EQLOCKINDIC pin signal goes up. The value of this signal can also be read through the I^2C-bus.

DAC interface

The TDA8960 D/A interface connects to an external off-chip serial D/A converter. It supports four different serial modes.

External interface

The DAC interface consists of pins 61 to 64; see Table 2.

Table 2 DAC interface

PIN	FUNCTION
TRSDO	serial data output
TRSTB	strobe signal which can be used by the DAC to shift in serial data
TRCS	chip select signal for DAC is also used by some DACs to load serially shifted data in the internal parallel register on the positive edge
TRLD	load signal used by some DACs to load serially shifted data in the internal parallel latches

Output modes

Table 3 shows which DACs can be used in the different output modes.

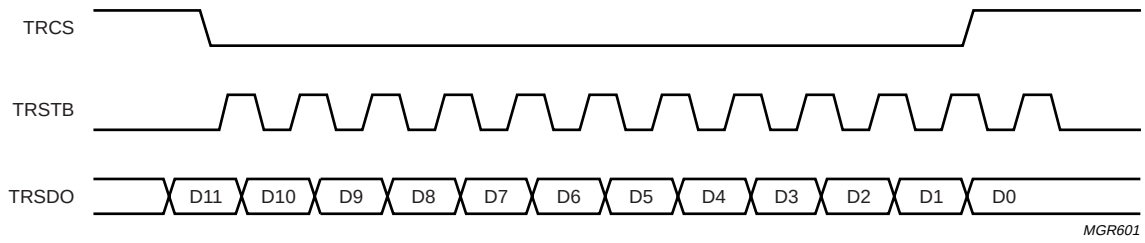
Table 3 DAC serial interface modes and DAC types

OUTPUT MODE	POLARITY	SET-UP TIME (ns)	EXAMPLE DEVICE
0	+dF/dV	67	Maxim MAX531, MAX538, MAX539, MAX504 and MAX515 Texas Instruments TLC5615 Sipex SP9500 and SP960 Linear Technology TLC1451
1	+dF/dV	45	Analog Devices AD7943
2	+dF/dV	45	Analog Devices DAC8512
3	–dF/dV	67	same types as mode 0

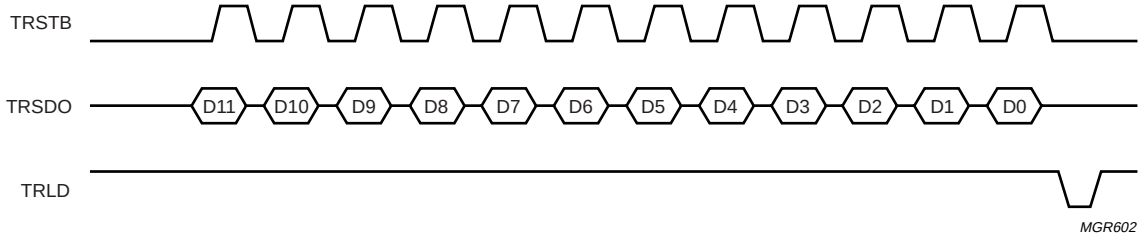
The operating mode is programmed by means of the I^2C-bus interface. Bits 4 and 5 of registers 09H control the mode; see Table 13.

The timing diagrams of the different serial modes are shown in Fig.4. Modes 0 and 3 do not use the load signal available at pin TRLD. In mode 3 the output of the timing recovery low-pass filter is inverted to control VCXOs which have a negative dF/dV. Modes 0 and 3 can provide up to 67 ns of the serial data set-up time from the moment the TRSDO output has a new data bit until the start of the TRSTB pulse.

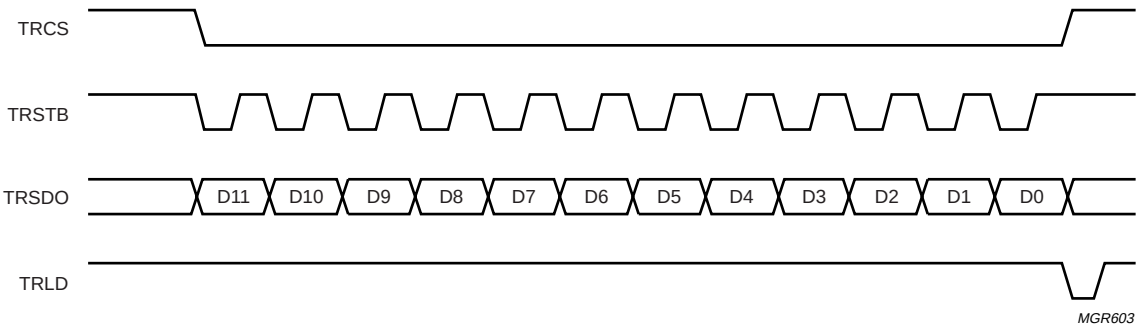
In mode 1 the TRCS pin is not used.



a. Modes 0 and 3



b. Mode 1



c. Mode 2

Fig.4 Timing diagrams of the different DAC serial interface modes.

Transport stream interface

The transport stream interface provides an output of 8-bit parallel MPEG-2 transport packets at a data rate of 5.38 Mbytes/s.

IMPLEMENTATION

The transport interface consists of a FIFO, which has two tasks:

1. Removal of the field sync segment from the generation of output data
2. Increase of the data rate of the de-randomizer from 2.69 to 5.38 MHz.

Basically the 208 bytes of a field segment (187 data bytes, 20 error correcting bytes and one segment sync byte) are distributed over the remaining 312 data segments.
The FIFO has a depth of two data segments. As the output data rate is 5.38 MHz we have to distribute 416 bytes, or two field sync data segments over 312 data segments. Every MPEG-2 transport packet corresponding to a data segment gets a delay equal to one 5.38 MHz clock cycle. Further, every third MPEG-2 transport packet gets an extra delay of one 5.38 MHz transport packet.

EXTERNAL INTERFACE

The transport stream consists of four signals and one data bus as shown in Table 4.

Table 4 Transport stream interface

NAME	FUNCTION
DATACLK	output clock
DATAVALID	valid demodulator output data or one valid MPEG transport packet
DATA[7 to 0]	output data stream (8-bit wide output bus)
SOP	indicates the start of a packet. It goes HIGH at the start of a packet and remains HIGH during the first byte of the packet, the so called sync byte
ERROR	a transport packet error indicator, which is HIGH for each 188 byte transport packet in which the Reed Solomon decoder found more errors than it could correct

FUNCTIONAL DESCRIPTION

The timing of the transport stream interface signals is shown in Fig.5.

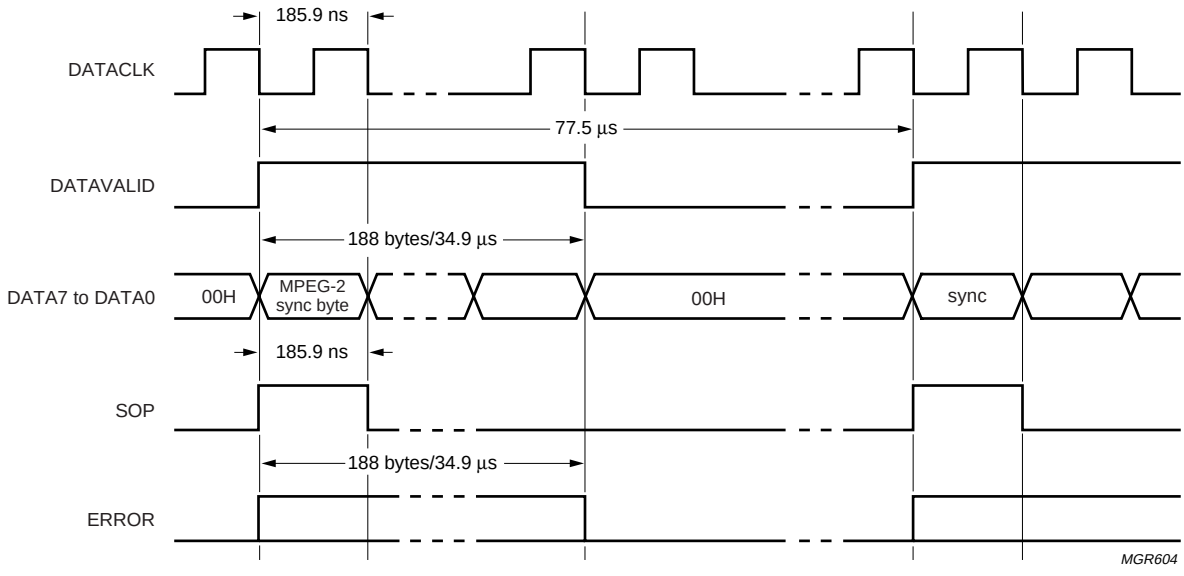


Fig.5 Timing diagram of the transport interface (normal mode).

The DATACLK signal is the 5.38 MHz demodulator output clock. It is derived from the system clock of 21.52 MHz. A few remarks can be made about the DATACLK signal:

- If a reset is applied, DATACLK becomes LOW; it remains LOW until reset is released and the symbol timing recovery block has detected the synchronization signals
- After a channel change the DATACLK signal stops; it starts again after the system has been locked on to a valid signal
- If the Reed Solomon decoder produces an invalid transport packet and the ERROR signal is asserted the DATACLK signal continues to change state
- If the sync recovery block is not able to detect the field sync or data segment sync, DATACLK will not change.

The DATAVALID signal indicates valid demodulator output data or one valid MPEG-2 transport packet. It is active HIGH for 188 bytes, or 34.9 μs. The zero bytes to be sent after the 188 valid bytes of the transport packet can be considered to be zeroed parity bytes.

SOP or start of packet signal is HIGH during the first byte of the packet.

The ERROR signal indicates that the transport packet contains uncorrectable output. The ERROR signal becomes HIGH in the following situations:

- If the Reed Solomon decoder is unable to correct all errors in a transport packet
- After a reset has been applied, the ERROR signal is asserted; it remains HIGH until a valid transport packet is produced by the demodulator
- If the demodulator is out of sync, thus can not detect the field sync and segment sync in the incoming data stream.

The ERROR signal can be asserted in the middle of a transport packet.

Sync byte and transport error indicator

The structure of a transport packet header is shown in Fig.6. For the VSB demodulator only the first two bytes of the so called transport packet header are important.

The first byte in each header of a transport packet is the so called MPEG-2 packet synchronization byte (sync byte). As specified in the MPEG-2 standard, this sync byte must have the same value for all packets. The VSB demodulator IC sets this byte for each outgoing transport packet to 47H.

The MSB of the second byte in the transport packet is the transport_error_indicator bit. It indicates that the Reed Solomon decoder was not able to correct all errors and the transport packet has invalid data.

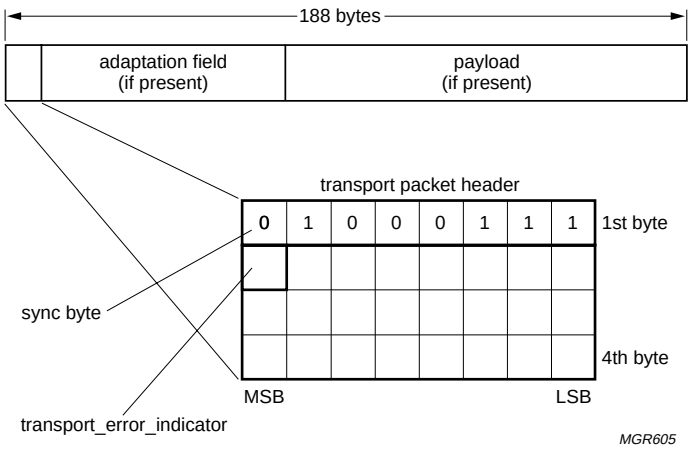


Fig.6 The structure of a transport packet header.

Boundary scan interface

The TDA8960 Test Access Port (TAP) conforms to *the "IEEE 1149.1 Joint Test Action Group (JTAG)"* standard. It is used for board level testing of integrated circuits and for testing the internals of an integrated circuit. The JTAG standard defines on-chip test logic, which consists of an instruction register, a group of test data registers including a bypass register and a boundary scan register, four dedicated pins collectively called the Test Access Port (TAP) and a TAP controller.

INSTRUCTION REGISTER

The instruction register consists of four bits without parity. There are five defined public instructions; see Table 5.

Table 5 Public instruction codes

INSTRUCTION	CODE	SELECTED DATA REGISTER
BYPASS(1)	1111	bypass (initialized state)
SAMPLE(2)	0001	boundary scan
EXTEST(3)	0000	boundary scan
INTEST(4)	0011	boundary scan
IDCODE(5)	0010	identification or bypass

Notes

1. The bypass instruction provides a minimum length (1-bit) serial path between the TDI and TDO pins when no test operation is required.
2. This instruction can be used to take a sample of the inputs and outputs during normal operation of the component. It can also be used to preload data values into the latched outputs of the boundary scan register.
3. This instructions allows testing off-chip circuitry and board level interconnections.
4. This instruction allows low speed, static testing of the on-chip logic. It can also be used after the chip is mounted on a printed circuit board.
5. This instruction will return the manufacturer ID, part number code and version code. For the TDA8960 the manufacturer ID is 'B00000010101', the part number code is 'SVSB' and the version code is 'D1'.

In addition three private instructions are implemented to control different test modes; see Table 6.

Table 6 Private instruction codes

INSTRUCTION	CODE	TEST MODE
SCAN_TEST	1000	test on-chip scan chains
BIST_TEST	1001	BIST test of de-interleaver RAM
RAM_TEST	1010	scan test of the on-chip memories
CHAR_MODE	1011	characterization mode

In the characterization mode the IC is scan-testable in the same way as in the scan test mode. However the outputs are not switched to the scan chain outputs. The outputs retain their functionality. It is now possible to scan test pattern through the logic and to verify if the timing constrains at the outputs are met.

EXTERNAL INTERFACE

The TAP consists of five pins as shown in Table 7.

Table 7 TAP external interface

SIGNAL	TYPE	DESCRIPTION
TMS	I	test mode select
TCK	I	test clock
TDI	I	test data input
TDO	O	test data output
TRST	I	test asynchronous reset

OPERATION

The TAP controller is a finite state machine. It selects a JTAG instruction or a data register to store the input based on the TMS signal, receives instructions and data on the TDI pin, executes the instruction when triggered by TMS, and shifts data out of TDO.

TCK provides the clock signal for the test logic required by the standard. TCK is asynchronous to the system clock. Stored devices in the JTAG controller must retain their state indefinitely when TCK is stopped at logic 0.

The signal received at TMS is decoded by the TAP controller to control test functions. The logic is required to sample TMS at the rising edge of TCK.

Serial test instructions and test data are received at TDI. The TDI signal is required to be sampled at the rising edge of TCK. When test data is shifted from TDI to TDO, the data must appear without inversion at TDO after a number of rising and falling edges of TCK, determined by the length of the instruction or test data register selected.

TDO is the serial output for test instructions and data from the TAP controller. Changes in the state of TDO must occur after the falling edge of TCK. This is because devices connected to TDO are required to sample TDO at the rising edge of TCK. The TDO driver must be in an inactive state (i.e. TDO line must be flat) except when the scanning of data is in progress.

I²C-bus interface

The I²C-bus interface is used to write control information to and read low-speed diagnostic information from the TDA8960. The key features of the I²C-bus interface are:

- I²C-bus data rate up to 400 kbits/s
- Support for only 7-bit addressing and the possibility of modifying the slave address externally.

A typical system using the I²C-bus interface is illustrated in Fig.7. The TDA8960 is connected as a slave to a master through SCL and SDA. Note that the bus has one pull-up resistor for each of the clock and data lines.

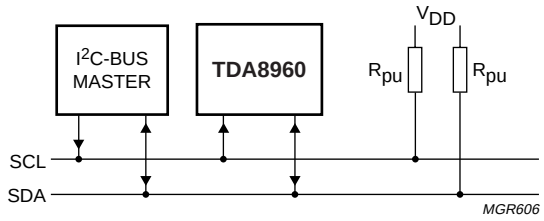


Fig.7 Typical I²C-bus system implementation.

EXTERNAL INTERFACE

The I²C-bus interface consists of four signals as shown in Table 8.

Table 8 I²C-bus external interface

SIGNAL	TYPE	DESCRIPTION
SDA	I/O	I²C-bus serial data
SCL	I	I²C-bus clock
A0	I	I²C-bus slave address bit 0
A1	I	I²C-bus slave address bit 1

The TDA8960 has 3.3 V I/O and I²C-bus pins. Therefore, in a complete system some circuitry might be necessary to allow ICs with different supply voltages to communicate and be controlled. This has been described in an application report available from Philips Semiconductors (application report *"AN97055"*, issued 1997 Aug 04).

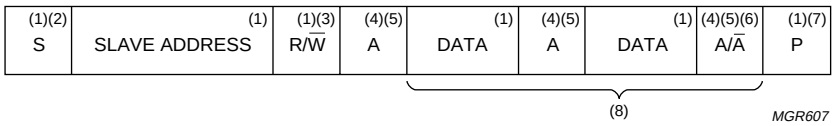
ADDRESSING THE DEVICE

Addressing the VSB demodulator over the system the I^{2}C-bus requires that the 7-bit slave address (A6 to A0) of the device is sent over the bus in accordance with the protocols, together with the R/$\overline{W}$ bit equal to logic 1 or 0 to write or read data respectively.

The slave address of the device is shown in Table 9. Bits 0 to 6 are predefined, but bits 0 and 1 can be set using the external pins A0 and A1.

Table 9 Slave address

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
0	0	0	1	1	A1	A0	0 = write 1 = read



(1) From master to slave
(2) S = START condition
(3) Logic 0 (write)
(4) From slave to master
(5) A = acknowledge (SDA LOW)
(6) $\overline{A}$ = not acknowledge (SDA HIGH)
(7) P = STOP condition
(8) Data transferred (n bytes + acknowledge).

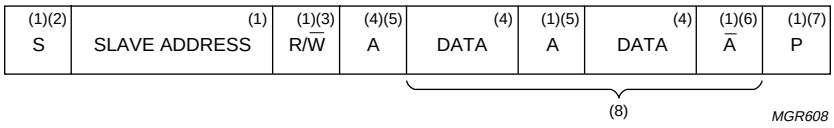
Fig.8 A master-transmitter addresses a slave receiver with a 7-bit address (write access).

A write operation is shown in Fig.8. After the START condition, the slave address followed by the R/$\overline{W}$ bit is transmitted. The receiver, the TDA8960, sends an acknowledge and the transmitter starts sending the register values. After each received byte, the TDA8960 sends an acknowledge. The transfer stops if the TDA8960 does not acknowledge the transfer and/or the master sends a STOP condition.

If register 08H has to be written to, eight consecutive bytes are written. The first corresponds to register 01H, the second to 02H and so on. The TDA8960 will auto-increment the accessed address automatically. Up to ten consecutive addresses can be written.

In Table 11 the default values are given for a number of reserved addresses and reserved bits of certain addresses. These correct default values have to be written in order to prevent unexpected behaviour of the IC.

Figure 9 shows a read operation. The master sends a START condition followed by the slave address and the R/$\overline{W}$ bit is set to logic 1. The slave returns an acknowledge followed by the value of the first address. The master sends another acknowledge and the next value of the address is returned. If the master transmits a STOP condition after the acknowledge, the transfer is stopped. Up to three consecutive addressed (00H to 03H) can be read.



(1) From master to slave.
(2) S = START condition.
(3) Logic 1 (read).
(4) From slave to master.
(5) A = acknowledge (SDA LOW).
(6) $\overline{A}$ = not acknowledge (SDA HIGH).
(7) P = STOP condition.
(8) Data transferred (n bytes + acknowledge).

Fig.9 A master-transmitter addresses a slave receiver with a 7-bit address (read access).

Table 10 I^2C-bus control register overview (write); note 1

FUNCTION	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
Operation	00H							GNRL_RST	INITIAL_RST
Reserved	01H								
Reserved	02H								
Operation	03H					AGC_THRES			
Reserved	04H								
Reserved	05H								
Reserved	06H								
Reserved	07H								
Carrier recovery	08H					AD_FMT	CR_INV		
Timing recovery	09H			INTMOD					

Note

1. Do not write past address 09H.

Table 11 I^2C-bus control registers (default settings after reset)

FUNCTION	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
Operation	00H	0	0	0	0	0	0	0	0
Reserved	01H	0	0	0	0	0	0	0	0
Reserved	02H	0	0	0	0	0	1	0	0
Operation	03H	0	0	0	0	0	0	0	0
Reserved	04H	0	0	0	0	0	0	1	0
Reserved	05H	1	0	0	0	0	0	0	0
Reserved	06H	0	0	0	0	0	0	0	0
Reserved	07H	1	1	0	0	1	0	1	0
Carrier recovery	08H	0	0	0	0	0	1	0	0
Timing recovery	09H	0	0	0	0	0	0	0	0

Table 12 I²C-bus diagnostic registers overview (read); note 1

FUNCTION	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
Operation	00H						LOCK_INDICATOR	EQ_LOCK_INDICATOR	
Equalizer	01H	MSE[15 to 8]							
	02H	MSE[7 to 0]							
Carrier recovery	03H	CR_OFFSET[7 to 0]							

Note

1. Do not read past address 03H.

Table 13 I²C-bus control registers (write); notes 1 and 2

ADDRESS	FUNCTION	COMMENTS	BIT	FIELD NAME	VALUE
00H	operation	reserved	7 to 2		
		general reset (note 1)	1	GNRL_RESET	0 = disable
					1 = enable
		initial reset (note 2)	0	INITIAL_RESET	0 = disable
					1 = enable
03H	operation	reserved	7 to 4		
		AGC threshold value	3 to 0	AGC_THRES	
08H	carrier recovery	reserved	7 to 4		
		A/D input format	3	AD_FMT	0 = twos complement
					1 = binary
		inverted spectrum	2	CR_INV	0 = pilot at 8.07 MHz
					1 = pilot at 2.69 MHz
		reserved	1 to 0		
09H	timing recovery	reserved	7 to 6		
		DAC interface mode	5 to 4	INT_MOD	00 = mode 0 (TRLD not used)
					01 = mode 1 (TRCS not used)
					10 = mode 2 (TRCS and TRLD are used)
					11 = mode 3 (TRLD not used; negative dF/dV
		reserved	3 to 0		

Notes

1. Operating modes and control parameters are reset to their initial values.
2. Operating modes and control parameters are not affected.

Table 14 I^2C-bus diagnostic registers (read)

ADDRESS	FUNCTION	COMMENTS	BIT	FIELD NAME
00H	operation	reserved	7 to 3	
		sync recovery lock indicator	2	LOCK_INDICATOR
		equalizer lock indicator	1	EQ_LOCK_INDICATOR
		reserved	0	
01H	equalizer	equalizer mean square error value	15 to 8	MSE
02H			7 to 0	MSE
03H	carrier recovery	carrier recovery offset	7 to 0	CR_OFFSET

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_I	input voltage on any pin with respect to digital ground (V_{SSD})		–0.5	–	V_{DDD} + 0.5	V
I_I	DC current into any input		–	–	tbf	mA
I_O	DC current out of any output		–	–	tbf	mA
T_j	junction temperature		0	–	105	°C
T_{stg}	storage temperature		–	–	–	°C
T_{amb}	ambient temperature		–20	+25	+70	°C
P_{tot}	total power dissipation		–	1.0	–	W
V_{es}	electrostatic handling	note 1	–3000	–	+3000	V
		note 2	–300	–	+300	V

Notes

1. Human body model: C = 100 pF; R = 1.5 kΩ; 3 zaps positive and 3 zaps negative.
2. Machine model: C = 200 pF; L = 0.5 μH; R = 10 Ω; 3 zaps positive and 3 zaps negative.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	55	K/W

DC CHARACTERISTICS

V_{DDD} = 3.3 V; V_{SSD} = 0 V; T_{amb} = 25 °C; unless otherwise specified; note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
I_{DDD}	digital supply current		–	300	–	mA
Inputs						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	–	V
I_{LI}	input leakage current		–	–	1	μA
C_i	input capacitance		8	–	25	pF
Output						
V_{OL}	LOW-level output voltage		–	–	0.4	V
V_{OH}	HIGH-level output voltage		2.4	–	–	V
I_{OL}	LOW-level output current		–	–	4	mA
3-state output, pin AGCOUT						
$I_{O(Z)}$	high-impedance output current		–	–	1	μA
$C_{O(Z)}$	high-impedance output capacitance		–	–	100	pF
I^2C-bus, pins SDA and SCL						
V_{IL}	LOW-level input voltage		–0.5	–	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	–	V_{DDD} + 0.5	V
V_{OL}	LOW-level output voltage		0	–	0.4	V
V_{OH}	HIGH-level output voltage	note 2	–	–	3.3	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	–	–	mA
I_L	leakage current	$V_I = V_{SSD}$ or V_{DDD}	–	–	±10	μA
C_i	input capacitance	$V_I = V_{SSD}$	–	–	8	pF

Notes

1. All supply connections must be made to the same external power supply unit.
2. Open-drain output, determined by V_{DDD} via an external pull-up resistor.

AC CHARACTERISTICS

V_{DDD} = 3.3 V; V_{SSD} = 0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock (pin CLK)						
$f_{clk(sys)}$	system clock frequency		–	21.52	–	MHz
t_{CLKH}	system clock HIGH time		–	21.23	–	ns
t_{CLKL}	system clock LOW time	note 1	–	21.23	–	ns
A/D interface (pins ADIN[9 to 0])						
$t_{su(A/D)}$	A/D interface set-up time		5	–	–	ns
$t_{h(A/D)}$	A/D interface hold time		5	–	–	ns
DAC interface (pins TRSDO, TRCS, TRLD and TRSTB); see Fig.13						
$t_{su(D/A)}$	D/A interface set-up time		–	40	–	ns
$t_{h(D/A)}$	D/A interface hold time		–	0	–	ns
Transport stream interface (pins DATA[7 to 0], SOP, ERROR and DATAVALID); see Fig.14						
$t_{su(D)}$	transport interface data set-up time		5	–	–	ns
$t_{h(D)}$	transport interface data hold time		5	–	–	ns
$t_{DATACLKL}$	transport interface DATACLK LOW time		180	–	–	ns
$t_{DATACLKH}$	transport interface DATACLK HIGH time		180	–	–	ns
$t_{DATCLKW}$	transport interface DATACLK period		371.7	–	–	ns
$t_{DAT-VAL}$	transport interface DATA to DATAVALID, ERROR and SOP		0	–	–	ns
I^2C-bus (pins SDA and SCL); see Fig.10						
f_{SCL}	SCL clock frequency		0	–	400	kHz
t_{BUF}	bus free time between a STOP and START condition		1.3	–	–	µs
$t_{HD;STA}$	hold time (repeated) START condition; after this period the first clock pulse is generated		0.6	–	–	µs
t_{LOW}	LOW period of the SCL clock		1.3	–	–	µs
t_{HIGH}	HIGH period of the SCL clock		0.6	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
$t_{HD;DAT}$	data hold time		0	–	0.9	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
t_{SP}	pulse width of spikes which must be suppressed by the input filter		tbf	–	tbf	ns
t_r	rise time of both SDA and SCL signals	note 2	$20 + 0.1C_b$	–	300	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_f	fall time of both SDA and SCL signals	note 1	$20 + 0.1C_b$	–	300	ns
C_b	capacitive load for each bus line		–	–	400	pF
JTAG interface (pins TDO, TDI, TCK, TMS and TRST); see Fig.11						
$t_{d(TCK-TDO)}$	pin TCK to TDO valid delay		2	–	10	ns
$t_{su(i)(TCK)}$	input set-up time to TCK		10	–	–	ns
$t_{h(i)(TCK)}$	input hold time from TCK		2	–	–	ns
Reset (pin RSTAN)						
$t_{su(PO)L}$	power-on set-up time LOW		23	–	–	ns

Notes

1. The chip clock (CLK) comes from a VXCO controlled by the external DAC. The control loop keeps the clock signal constant at a frequency twice the symbol rate.
2. C_b = total capacitance of one bus line in pF.

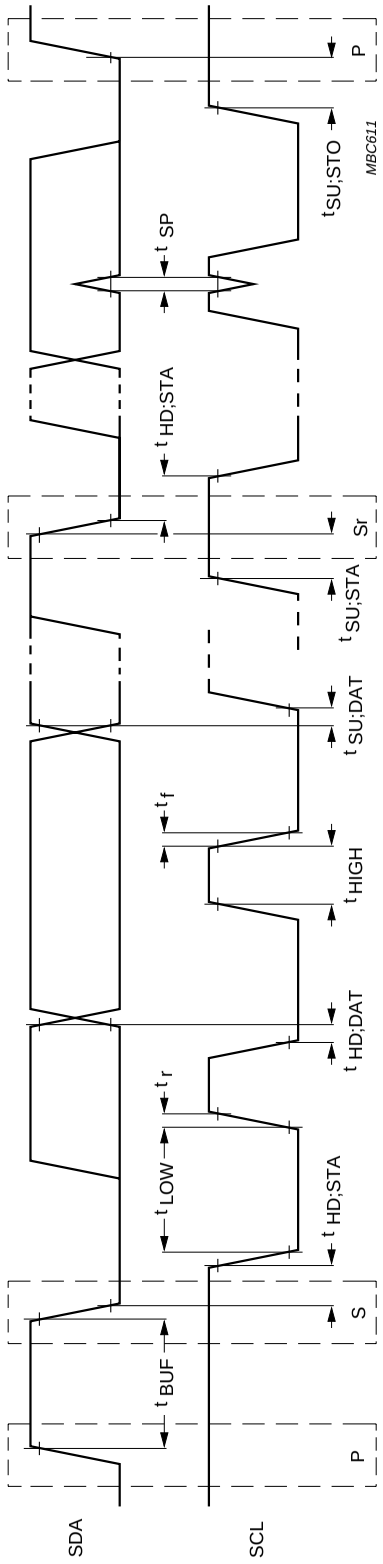


Fig.10 I²C-bus timing diagram.

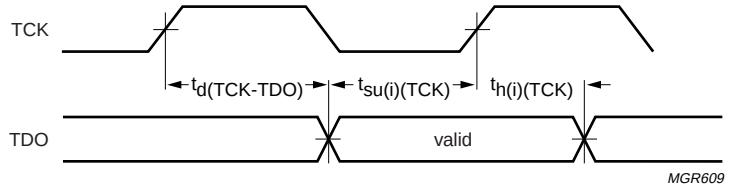
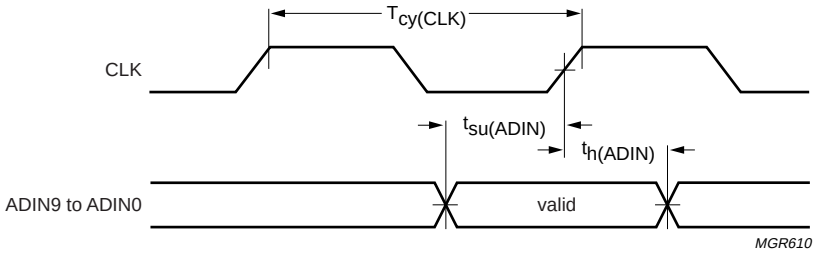


Fig.11 JTAG I/O timing.



$T_{cy(clk)}$ = 46.47 ns.

Fig.12 Input timing.

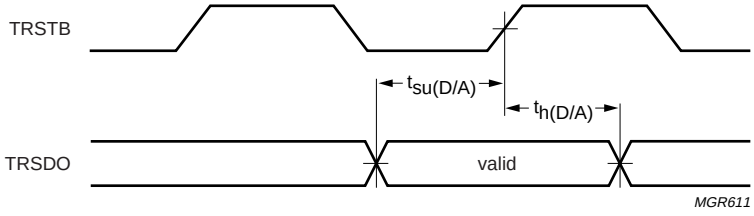


Fig.13 Serial D/A converter interface I/O timing.

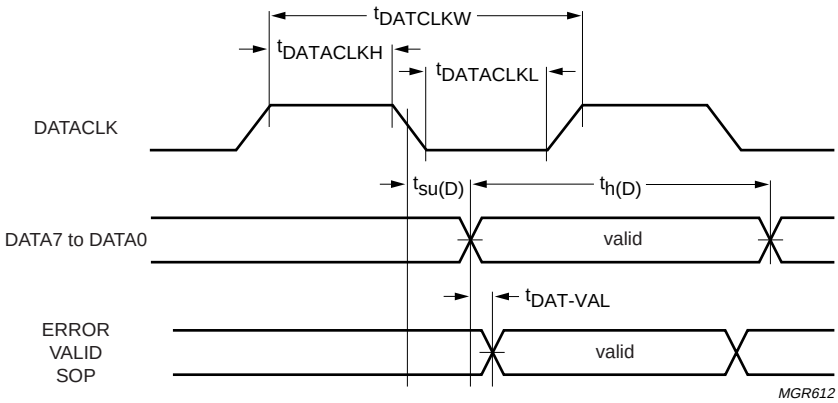


Fig.14 Transport interface timing.

APPLICATION INFORMATION

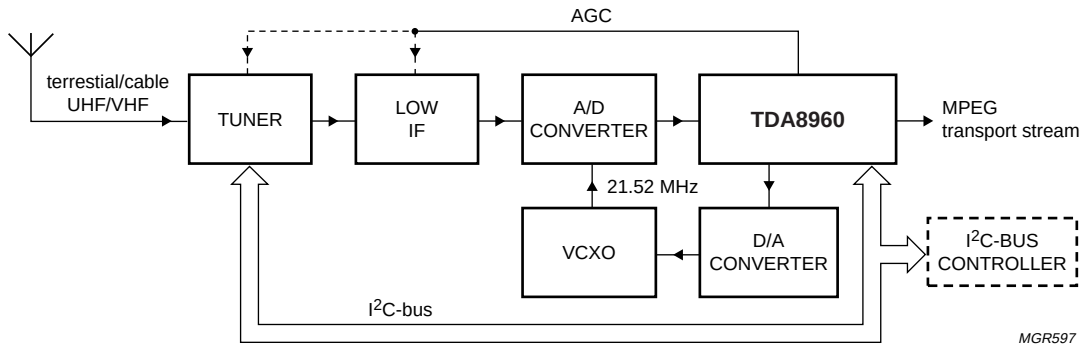
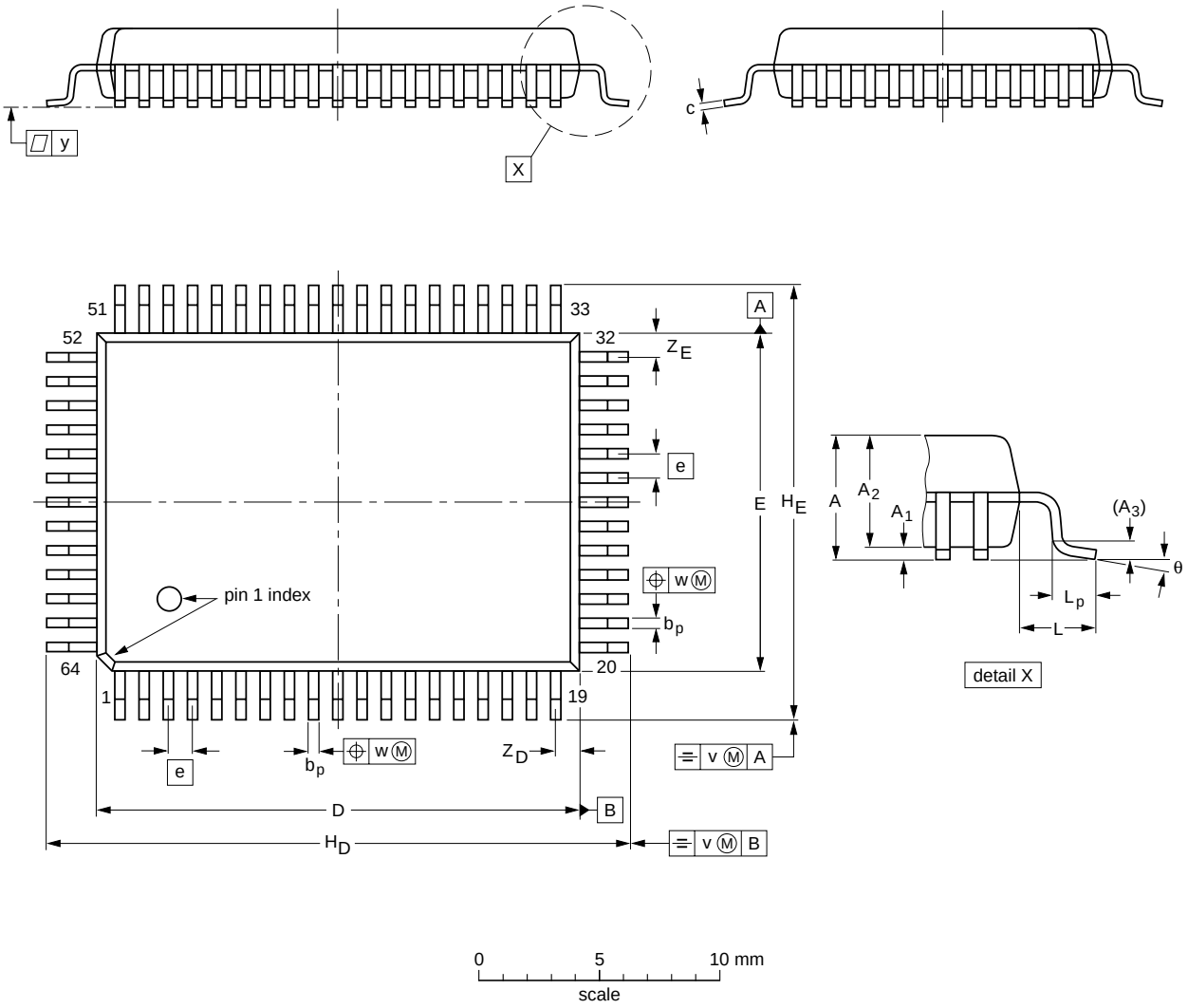


Fig.15 Front-end unit for reception of 8-VSB signals.

PACKAGE OUTLINE

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT319-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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Information as of 2000-08-20

TDA8960; ATSC 8-VSB demodulator and decoder

Description

The TDA8960 is an ATSC-compliant demodulator and forward error correction decoder for reception of 8-VSB modulated signals for terrestrial and cable applications:

- **Terrestrial:** reception of 8-VSB modulated signals via standard 6 MHz VHF/UHF terrestrial TV channels (TV channels 2 to 69 in the United States)
- **Cable:** reception of 8-VSB modulated signals via standard 6 MHz VHF/UHF cable TV channels.

Most of the loop components needed to recover the data from the received symbols are internal. The only required external loop components are a low-speed serial D/A converter and a Voltage Controlled crystal Oscillator (VCXO) for the symbol timing recovery and an opamp integrator for the AGC. Loop parameters of the clock and carrier recovery can be controlled by the I²C-bus.

A tuner converts the incoming RF frequency to a fixed IF frequency centred at 44 MHz. The output of the tuner is filtered, followed by a down conversion in an IF block to a low IF frequency centred at 1/2 the VSB symbol rate (or a frequency of approximately 5.38 MHz). The low IF signal is applied to the A/D converter.

To use its full input span, the A/D converter is located within what is typically a fine AGC loop which includes a variable gain stage at the output of the IF block. However, it is also possible to apply the TDA8960 AGC control output directly to the tuner. The detector for the TDA8960 AGC output is located after the A/D converter and determines the peak level of the incoming signals. After gain control, the low IF signal is sampled at a nominal rate of twice the VSB symbol frequency, or approximately 21.5 MHz.

The carrier recovery is performed completely internally. This function consists of a digital frequency and Frequency Phase-Locked Loop (FPLL).

Data shaping is performed with a square root raised cosine (half Nyquist) filter with roll-off factor of 11.5%.

Symbol timing recovery is performed mostly within the TDA8960, except that a low cost D/A converter and VCXO are required externally to generate the nominal 21.52 MHz clock signal for the A/D converter and TDA8960.

After carrier recovery, half Nyquist filtering and symbol timing recovery, adaptive equalization is performed based on the use of the ATSC field sync (trained equalization) and/or the 8-VSB data itself (blind equalization). The adaptive equalizer uses a DFE structure.

After trellis decoding, the stream is de-interleaved with a convolutional de-interleaver (interleaving depth 52). The memory for de-interleaving is on-chip. The Reed Solomon decoder is ATSC-compliant with a length of 207 and can correct up to 10 bytes. The decoded stream is de-randomized using a Pseudo Random Bit Sequence (PRBS). Finally the data is passed to a First-In, First-Out (FIFO) register that prevents the appearance of irregular gaps in the output data.

The output of the TDA8960 is an ATSC-compliant MPEG-2 packet stream together with a clock. Furthermore some signal flags are provided to indicate the sync bytes and the valid data bytes. Uncorrected blocks are also indicated.

The 8-bit wide MPEG-2 stream can be applied to an MPEG-2 transport demultiplexer.

Features

General features

- One-chip Advanced Television Systems Committee (ATSC)-compliant demodulator and concatenated trellis (Viterbi)/Reed Solomon decoder with de-interleaver and de-randomizer
- 0.4 µm process
- 3.3 V device
- 64-lead QFP64 package
- Boundary scan test
- Output format: 8-bit wide bus.

8-VSB demodulator

- On-chip digital circuitry for tuner Automatic Gain Control (AGC)
- Square root raised cosine filter with 11.5% roll-off factor
- Fully internal carrier recovery loop
- Mostly internal clock recovery and AGC loops with programmable loop filters
- External indication of demodulator lock.

Adaptive equalizer

- Feed forward including a Decision Feedback Equalizer (DFE) structure:
- Range of -2.3 to +10.5 &#s
- Adaptation based on ATSC field sync (trained) and/or 8-VSB data (blind)
- Trellis (Viterbi) decoder
- Rate 2/3 (Rate 1/2 Ungerboeck code based).

Reed Solomon decoder

- (207, 187 and T = 10) Reed Solomon code
- Internal convolutional de-interleaving (I = 52; using internal memory)
- External indication of uncorrectable error; transport error indicator bit in Motion Picture Export Group (MPEG) packet header is also set
- Followed by de-randomizer based on ATSC standard.

I²C-bus interface

- I²C-bus interface to initialize and monitor the demodulator and Forward Error Correction (FEC) decoder. Operation without I²C-bus control is possible (default).

Applications

- Digital ATSC compliant TV receivers
- Personal computers with digital television capabilities
- Set-top boxes.

Datasheet

Type nr.	Title	Publication release date	Datasheet status	Page count	File size (kB)	Datasheet
TDA8960	ATSC 8-VSB demodulator and decoder	14-Jun-99	Preliminary Specification	32	126	Download

Products, packages, availability and ordering

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